Listing of Claims:

Claims 1-4 (cancelled)

Claim 5 (new): Apparatus for generating a plurality of control clocks in response to a power state of a plurality of processing units, comprising:

a first multiplexor for selectively outputting one of a DC level and a source clock in response to a power down signal;

a branch for branching the output of the first multiplexor into a predetermined number of branches; and

a plurality of multiplexors, each for selecting respective ones of the clock signals from the branch and the DC level in response to the power state of a corresponding one of the plurality of processing units and outputting the selected signal to the corresponding processing unit.

Claim 6 (new): The Apparatus as recited in claim 5, further comprising a logic device for AND operating the outputs of the plurality of multiplexors to drive a memory device.

Claim 7 (new): A signal processing system for reducing power consumption, comprising:

a plurality of processing units;

an internal clock signal generator unit for receiving a source clock and a power down signal and generating clock signals, each of the clock signals corresponding to a respective one of the plurality of processing units.

Claim 8 (new): The signal processing system as recited in claim 7, wherein the internal clock signal generator unit includes:

a first multiplexor for selectively outputting one of a DC level and the source clock in response to the power down signal;

a branch for branching the output of the first multiplexor into a predetermined number of branches; and

second, third and fourth multiplexors, each for selecting respective ones of the clock signals from the branch and the DC level in response to the power state of a

corresponding one of the bit stream processing unit, the digital signal processing unit and to post processing unit, each of the second, third and fourth multiplexors outputting, a selected signal to a respective one of the bit stream processing, digital signal processing and post processing units to output the selected signal to the corresponding processing unit.

Claim 9 (new): The system as recited in claim 8, wherein the internal clock signal generator unit includes a logic device for AND operating the outputs of the plurality of multiplexors to drive a memory device.